Intel Instruction Set Extensions

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Intel Transactional Synchronization Extensions (Intel TSX) comes in two flavours: HLE and RTM. TSX-NI is an extension (RTM) to previous instruction set (HLE).

Recent processor architectures such as Intel Westmere (and later) support Instruction Set Extensions, KECCAK, ARM NEON, SIMD, and SHA3. Intel's investment in instruction set innovation over the past 40 years has enabled the Intel SSE2 extensions and the Intel® NetBurst® microarchitecture.

Popular families, such as x86-64 or ARM, have processors supplied by Single Instruction Multiple Data (SIMD) instruction set extensions: SSE2, SSE3, SSSE3. MMX is officially a meaningless initialism trademarked by Intel, unofficially, the initials have been variously explained as standing for MultiMedia eXtension. ARM guns for high-performance computing with its new vector instruction set for a new type of scaling vector instruction, dubbed scalar vector extensions (SVE).

Both AMD and Intel support the AVX instruction set, but AMD's Steamroller. At the time of its initial release, the Intel SHA Extensions were seen as the logical next step to the 2008 AES-NI instruction set, and developers expected them.

Intel x86 Instruction Sets. Interruptions SSE is an SIMD instruction set extension to the x86 Registers available in the x86 instruction set (x86, Wikipedia).

Side-Channel Protections for Cryptographic Instruction Set Extensions provide a specific example with Intel's AES-NI cryptographic instruction set extensions.

Bit Manipulation Instructions Sets (BMI sets) are extensions to the x86 instruction set architecture for microprocessors from Intel and AMD. The purpose of these. Intel introduced an instruction set extension with the Intel® Pentium® III processor called Intel® Streaming SIMD Extensions (Intel® SSE), which was a major. We introduce Intel® Software Guard Extensions (Intel® SGX) SGX2 which extends the SGX instruction set to include dynamic memory management support.

This reference is intended to be precise opcode and instruction set reference is empty because the instruction doesn't belong to any instruction set extension. Use of processor-specific instruction set extensions. Tuning parameters Core 2 Kentsfield. 04-P4P. Intel Pentium 4 Prescott. SSE, SSE2, SSE3. 00-x86. none. Yes Intel® VT-x with Extended Page Tables (EPT) ‡ Yes Intel® TSX-NI Yes Intel® 64 ‡ Yes Instruction Set 64-bit. Instruction Set Extensions SSE4.1/4.2, AVX 2.0.